CLAIMS:

1. A method for forming graded junction regions operatively adjacent a transistor gate of CMOS circuitry, the method comprising the following steps:

providing a semiconductor material wafer;

defining a PMOS region and an NMOS region of the wafer;

providing a PMOS transistor gate over the PMOS region and providing an NMOS transistor gate over the NMOS region, the transistor gates having opposing lateral sidewalls;

providing sidewall spacers adjacent the sidewalls of the transistor gates, the sidewall spacers having a lateral thickness and comprising a sidewall spacer material;

providing a masking layer over the PMOS region;

after providing the masking layer over the PMOS region, and after providing the sidewall spacers adjacent the NMOS transistor gate, implanting an n-type conductivity-enhancing dopant into the semiconductor wafer to form electrically conductive NMOS source/drain regions within the semiconductor material operatively adjacent the NMOS transistor gate;

after forming the electrically conductive NMOS source/drain regions, etching the sidewall spacer material adjacent the NMOS transistor gate to remove only a portion of said spacer material and to thereby decrease the lateral thickness of the sidewall spacers adjacent the NMOS transistor gate; and

after decreasing the lateral thickness of the sidewall spacers adjacent the NMOS transistor gate, implanting a p-type conductivity-enhancing dopant into the semiconductor material to form halo regions operatively adjacent the NMOS source/drain regions.

2. The method of claim 1 further comprising, after providing transistor gates over the PMOS region and NMOS region, and prior to providing sidewall spacers adjacent the sidewalls of the transistor gates, forming NMOS LDD regions operatively adjacent the NMOS transistor gate.

3. The method of claim 1 further comprising:

after forming the electrically conductive NMOS source/drain regions, and prior to etching the sidewall spacer material adjacent the NMOS transistor gate, stripping the masking layer from over the PMOS region;

etching the sidewall spacer material adjacent the PMOS transistor gate to decrease the lateral thickness of the sidewall spacers adjacent the PMOS transistor gate; and

after decreasing the lateral thickness of the sidewall spacers adjacent the NMOS transistor gate and the PMOS transistor gate, blanket implanting the p-type conductivity-enhancing dopant into the semiconductor material of both the PMOS region and the NMOS region to form halo regions operatively adjacent the NMOS transistor gate and to form PMOS LDD regions operatively adjacent the PMOS transistor gate.

4. The method of claim 3 further comprising, prior to decreasing the lateral thickness of the sidewall spacers adjacent the PMOS transistor gate and subsequent to stripping the masking layer from over the PMOS region, forming electrically conductive PMOS source/drain regions within the semiconductor material operatively adjacent the PMOS transistor gate.

5. The method of claim 1 further comprising, prior to providing the masking layer over the PMOS region, forming PMOS LDD regions operatively adjacent the PMOS transistor gate.

6. The method of claim 1 wherein the semiconductor material wafer comprises an overall planar global configuration, the planar global configuration establishing a virtual planar top surface and an axis normal to the virtual planar top surface, and wherein the p-type conductivity-enhancing dopant is implanted at an angle other than parallel to the axis normal to the virtual planar top surface.

7. The method of claim 1 further comprising:

prior to providing the masking layer over the PMOS region, forming PMOS LDD regions operatively adjacent the PMOS transistor gate;

after forming the electrically conductive NMOS source/drain regions, and prior to etching the sidewall spacer material adjacent the NMOS transistor gate, stripping the masking layer from over the PMOS region;

etching the sidewall spacer material adjacent the PMOS transistor gate to decrease the lateral thickness of the sidewall spacers adjacent the PMOS transistor gate; and

after decreasing the lateral thickness of the sidewall spacers adjacent the NMOS transistor gate and the PMOS transistor gate, blanket implanting the p-type conductivity-enhancing dopant into the semiconductor material of both the PMOS region and the NMOS region to form halo regions operatively adjacent the NMOS transistor gate and to enhance the conductivity of the PMOS LDD regions.

8. The method of claim 1 wherein the semiconductor material wafer comprises an overall planar global configuration, the planar global configuration establishing a virtual planar top surface and an axis normal to the virtual planar top surface, and further comprising:

after forming the electrically conductive NMOS source/drain regions, and prior to etching the sidewall spacer material adjacent the NMOS transistor gate, stripping the masking layer from over the PMOS region;

etching the sidewall spacer material adjacent the PMOS transistor gate to remove only a portion of said spacer material and to thereby decrease the lateral thickness of the sidewall spacers adjacent the PMOS transistor gate; and

after decreasing the lateral thickness of the sidewall spacers adjacent the NMOS transistor gate and the PMOS transistor gate, blanket implanting the p-type conductivity-enhancing dopant at an angle other than parallel to the axis normal to the virtual planar top surface to form NMOS halo regions operatively adjacent the NMOS transistor gate and to form PMOS LDD regions operatively adjacent the PMOS transistor gate.

9. The method of claim 1 wherein the portion of spacer material removed from the sidewall spacers constitutes no more than about 90% of the lateral thickness of the sidewall spacers adjacent the NMOS transistor gate.

10. The method of claim 1 wherein the sidewalls of the transistor gates comprise polysilicon, the method further comprising:

prior to providing sidewall spacers adjacent the sidewalls, oxidizing the polysilicon of the sidewalls.

11. The method of claim 10 further comprising, prior to providing sidewall spacers adjacent the sidewalls of the NMOS transistor gate, forming NMOS LDD regions operatively adjacent the NMOS transistor gate.

12. CMOS circuitry comprising at least one transistor formed by the method of claim 1.

13. A method for forming graded junction regions operatively adjacent a transistor gate, the method comprising the following steps:

providing a semiconductor material wafer;

providing a transistor gate over the semiconductor material wafer, the transistor gate having opposing lateral sidewalls;

providing sidewall spacers adjacent the sidewalls of the transistor gate, the sidewall spacers having a lateral thickness and comprising a sidewall spacer material;

after providing the sidewall spacers, implanting a first conductivity-enhancing dopant into the semiconductor wafer to form electrically conductive source/drain regions within the semiconductor material operatively adjacent the transistor gate;

after forming the electrically conductive source/drain regions, etching the sidewall spacer material to remove only a portion of said spacer material and to thereby decrease the lateral thickness of the sidewall spacers; and

after decreasing the lateral thickness of the sidewall spacers, implanting a second conductivity-enhancing dopant into the semiconductor material to form graded junction regions operatively adjacent the source/drain regions.

14. The method of claim 13 wherein the semiconductor material wafer comprises an overall planar global configuration, the planar global configuration establishing a virtual planar top surface and an axis normal to the virtual planar top surface, and wherein the second conductivity-enhancing dopant is implanted at an angle other than parallel to the axis normal to the virtual planar top surface.

15. The method of claim 13 wherein the transistor is a PMOS transistor, the second conductivity-enhancing dopant is a p-type dopant, and the implant of the second conductivity-enhancing dopant forms LDD regions operatively adjacent the PMOS source/drain regions.

16. The method of claim 13 wherein the transistor is a PMOS transistor, the second conductivity-enhancing dopant is an n-type dopant, and the implant of the second conductivity-enhancing dopant forms halo regions operatively adjacent the PMOS source/drain regions.

17. The method of claim 16 wherein the second conductivity-enhancing dopant comprises phosphorus.

18. The method of claim 13 wherein the transistor is an NMOS transistor, the second conductivity-enhancing dopant is a p-type dopant, and the implant of the second conductivity-enhancing dopant forms halo regions operatively adjacent the NMOS source/drain regions.

19. The method of claim 18 wherein the second conductivity-enhancing dopant comprises boron.

20. The method of claim 13 wherein the transistor is an NMOS transistor, the second conductivity-enhancing dopant is a n-type dopant, and the implant of the second conductivity-enhancing dopant forms LDD regions operatively adjacent the NMOS source/drain regions.

21. A transistor formed by the method of claim 13.

22. A method for implanting graded junction regions into a peripheral NMOS transistor and source/drain regions into a memory array of NMOS transistors, the method comprising the following steps:

providing a semiconductor material wafer;

defining a memory array region of the wafer;

defining a PMOS region and a peripheral NMOS region of the wafer;

providing a PMOS transistor gate over the PMOS region, providing a peripheral NMOS transistor gate over the peripheral NMOS region, and providing an array of memory NMOS transistor gates over the memory array region, the transistor gates having opposing lateral sidewalls;

providing sidewall spacers adjacent the sidewalls of the transistor gates, the sidewall spacers having a lateral thickness and comprising a sidewall spacer material;

providing a masking layer over the PMOS region and over the memory array region;

after providing the masking layer over the PMOS region and the memory array region, and after providing the sidewall spacers adjacent the peripheral NMOS transistor gate, implanting an n-type conductivity-enhancing dopant into the semiconductor wafer to form electrically conductive peripheral NMOS source/drain regions within the semiconductor material operatively adjacent the peripheral NMOS transistor gate;

after forming the electrically conductive NMOS source/drain regions, etching the sidewall spacer material adjacent the peripheral NMOS transistor gate to remove only a portion of said spacer material and to thereby decrease the lateral thickness of the sidewall spacers adjacent the peripheral NMOS transistor gate; and

after decreasing the lateral thickness of the sidewall spacers adjacent the peripheral NMOS transistor gate, implanting p-type conductivity-enhancing dopant into the semiconductor material to form halo regions operatively adjacent the peripheral NMOS source/drain regions.

23. The method of claim 22 further comprising, after providing transistor gates over the peripheral NMOS region and over the memory array region, and prior to providing sidewall spacers adjacent the sidewalls of the transistor gates, providing LDD regions operatively adjacent the peripheral NMOS transistor gate and providing memory gate source/drain regions operatively adjacent the memory NMOS transistor gates.

24. The method of claim 22 further comprising:

after forming halo regions operatively adjacent the NMOS source/drain regions, stripping the masking layer from over the PMOS region and providing a masking layer over the peripheral NMOS region;

after providing the masking layer over the NMOS region, etching the sidewall spacer material adjacent the PMOS transistor gate to decrease the lateral thickness of the sidewall spacers adjacent the PMOS transistor gate; and

after decreasing the lateral thickness of the sidewall spacers adjacent the PMOS transistor gate, implanting n-type conductivity-enhancing dopant into the semiconductor material to form halo regions operatively adjacent the PMOS transistor gate.

25. The method of claim 24 further comprising, prior to decreasing the lateral thickness of the sidewall spacers adjacent the PMOS transistor gate and subsequent to stripping the masking layer from over the PMOS region, forming electrically conductive PMOS source/drain regions within the semiconductor material operatively adjacent the PMOS transistor gate.

26. The method of claim 22 further comprising:

after forming halo regions operatively adjacent the NMOS source/drain regions, stripping the masking layer from over the PMOS region and providing a masking layer over the peripheral NMOS region;

after providing the masking layer over the NMOS region, etching the sidewall spacer material adjacent the PMOS transistor gate to decrease the lateral thickness of the sidewall spacers adjacent the PMOS transistor gate; and

after decreasing the lateral thickness of the sidewall spacers adjacent the PMOS transistor gate, implanting p-type conductivity-enhancing dopant into the semiconductor material to form LDD regions operatively adjacent the PMOS transistor gate.

27. The method of claim 26 further comprising, prior to decreasing the lateral thickness of the sidewall spacers adjacent the PMOS transistor gate and subsequent to stripping the masking layer from over the PMOS region, forming electrically conductive PMOS source/drain regions within the semiconductor material operatively adjacent the PMOS transistor gate.

28. The method of claim 22 further comprising:

after forming the electrically conductive peripheral NMOS source/drain regions, and prior to etching the sidewall spacer material adjacent the peripheral NMOS transistor gate, stripping the masking layer from over the PMOS region;

etching the sidewall spacer material adjacent the PMOS transistor gate to decrease the lateral thickness of the sidewall spacers adjacent the PMOS transistor gate; and

after decreasing the lateral thickness of the sidewall spacers adjacent the peripheral NMOS transistor gate and the PMOS transistor gate, blanket implanting the p-type conductivity-enhancing dopant into the semiconductor material of both the PMOS region and the NMOS region to form halo regions operatively adjacent the NMOS transistor gate and to form PMOS LDD regions operatively adjacent the PMOS transistor gate.

29. The method of claim 28 further comprising, prior to decreasing the lateral thickness of the sidewall spacers adjacent the PMOS transistor gate and subsequent to stripping the masking layer from over the PMOS region, forming electrically conductive PMOS source/drain regions within the semiconductor material operatively adjacent the PMOS transistor gate.

30. A semiconductor wafer comprising a peripheral NMOS and a memory array formed by the method of claim 22.

31. A method for forming graded junction regions operatively adjacent a transistor gate, the method comprising the following steps:

providing a semiconductor material wafer;

providing a transistor gate over the semiconductor material wafer, the transistor gate having opposing lateral sidewalls;

providing sidewall spacers adjacent the sidewalls of the transistor gate, the sidewall spacers having a lateral thickness and comprising a sidewall spacer material;

decreasing the lateral thickness of the sidewall spacers by removing only a portion of the sidewall spacers; and

after decreasing the lateral thickness of the sidewall spacers, implanting a conductivity-enhancing dopant into the semiconductor material to form graded junction regions operatively adjacent the transistor gate.

32. The method of claim 31 wherein the semiconductor material wafer comprises an overall planar global configuration, the planar global configuration establishing a virtual planar top surface and an axis normal to the virtual planar top surface, and wherein the second conductivity-enhancing dopant is implanted at an angle other than parallel to the axis normal to the virtual planar top surface.

33. The method of claim 31 further comprising, after providing the sidewall spacers and prior to decreasing the lateral thickness of the sidewall spacers, providing electrically conductive source/drain regions operatively adjacent the transistor gate.

34. The method of claim 31 further comprising incorporating the transistor gate into a PMOS transistor, wherein the implanted conductivity-enhancing dopant is a p-type dopant, and wherein the formed graded junction regions are LDD regions.

35. The method of claim 31 further comprising incorporating the transistor gate into a PMOS transistor, wherein the implanted conductivity-enhancing dopant is an n-type dopant, and wherein the formed graded junction regions are halo regions.

36. The method of claim 31 further comprising incorporating the transistor gate into an NMOS transistor, wherein the implanted conductivity-enhancing dopant is a p-type dopant, and wherein the formed graded junction regions are halo regions.

37. The method of claim 31 further comprising incorporating the transistor gate into an NMOS transistor, wherein the implanted conductivity-enhancing dopant is an n-type dopant, and wherein the formed graded junction regions are LDD regions.

38. A transistor formed by the method of claim 31.

39. A semiconductor transistor device comprising:

a region of a semiconductor material wafer;

a transistor gate over a portion of the region of the semiconductor material wafer, the transistor gate having opposing lateral sidewalls;

opposing source/drain regions operatively adjacent the transistor gate, each source/drain region having an inner lateral boundary;

opposing sidewall spacers adjacent the sidewalls of the transistor gate, each sidewall spacer having an outer lateral edge, the sidewall spacers and source/drain regions being paired such that the outer lateral edges of the sidewall spacers are displaced laterally inwardly relative to the inner lateral boundaries of the source/drain regions; and

lateral gaps, the lateral gaps extending from the outer lateral edges of the sidewall spacers to the inner lateral boundaries of the source/drain regions.

40. The device of claim 39 wherein the lateral gaps have a length, the length of the lateral gaps being from about 200 Angstroms to about 600 Angstroms.

41. The device of claim 39 further comprising graded junction regions inwardly adjacent the source/drain regions, the graded junction regions extending within the lateral gaps.

42. A method for forming a peripheral NMOS transistor and one or more memory NMOS transistors, the method comprising the following steps:

forming a peripheral NMOS transistor gate and one or more memory NMOS transistor gates;

forming source/drain regions, halo regions and LDD regions operatively adjacent the peripheral NMOS transistor gate, and forming source/drain regions operatively adjacent the one or more memory NMOS transistor gates, the steps of forming the regions occurring in a sequence such that one or more of the regions are formed last and are therefore last formed regions, wherein the LDD regions formed operatively adjacent the peripheral NMOS transistor gate are not the last formed regions; and

less than two masking layer provision steps after the formation of the LDD regions operatively adjacent the peripheral NMOS transistor gate, and prior to formation of the one or more last formed regions.

43. A method for forming graded junction regions operatively adjacent a transistor gate of CMOS circuitry, the method comprising the following steps:

providing a semiconductor material wafer;

defining a PMOS region and an NMOS region of the wafer;

providing a gate layer over the PMOS region and over the NMOS region;

patterning the gate layer over the NMOS region to form an NMOS transistor gate over the NMOS region while leaving the gate layer over the PMOS region unpatterned, the NMOS transistor gate having opposing lateral sidewalls;

providing sidewall spacers adjacent the sidewalls of the NMOS transistor gate, the sidewall spacers having a lateral thickness and comprising a sidewall spacer material;

after providing the sidewall spacers, forming electrically conductive NMOS source/drain regions within the semiconductor material operatively adjacent the NMOS transistor gate;

after forming the electrically conductive NMOS source/drain regions, etching the sidewall spacer material adjacent the NMOS transistor gate to remove only a portion of said spacer material and to thereby decrease the lateral thickness of the sidewall spacers; and

after decreasing the lateral thickness of the sidewall spacers adjacent the NMOS transistor gate, implanting conductivity-enhancing dopant into the semiconductor material to thereby form NMOS graded junction regions operatively adjacent the NMOS source/drain regions.

44. The method of claim 43 wherein the implanted conductivity-enhancing dopant is a p-type dopant and wherein the formed NMOS graded junction regions are halo regions.

45. The method of claim 43 wherein the portion of spacer material removed from the sidewall spacers constitutes no more than about 90% of the lateral thickness of the sidewall spacers adjacent the NMOS transistor gate.

46. The method of claim 43 wherein the gate layer comprises a polysilicon layer, a refractory metal layer over the polysilicon layer, an oxide layer over the refractory metal layer, and a silicon nitride layer over the oxide layer.

47. The method of claim 43 further comprising, after forming the NMOS transistor gate, and prior to providing sidewall spacers, forming NMOS LDD regions operatively adjacent the NMOS transistor gate.

48. The method of claim 43 wherein the opposing lateral sidewalls of the NMOS transistor gate comprise polysilicon, the method further comprising:

prior to providing sidewall spacers adjacent the NMOS transistor gate, oxidizing the polysilicon of the opposing lateral sidewalls to form an oxide layer along each opposing lateral sidewall.

49. The method of claim 48 further comprising, after forming the NMOS transistor gate, and prior to providing the oxide layer along each opposing lateral sidewall, forming NMOS LDD regions operatively adjacent the NMOS transistor gate.

50. The method of claim 43 wherein the semiconductor material wafer comprises an overall planar global configuration, the planar global configuration establishing a virtual planar top surface and an axis normal to the virtual planar top surface, and wherein the p-type conductivity-enhancing dopant is implanted at an angle other than parallel to the axis normal to the virtual planar top surface.

51. The method of claim 43 further comprising:

after forming the NMOS transistor gate, patterning the gate layer over the PMOS region to form a PMOS transistor gate over the PMOS region.

52. A method for implanting graded junction regions into a peripheral NMOS transistor and into a memory array of NMOS transistors, the method comprising the following steps:

providing a semiconductor material wafer;

defining a memory array region, a PMOS region and a peripheral NMOS region of the wafer;

providing a gate layer over the PMOS, peripheral NMOS and memory array regions;

patterning the gate layer over the peripheral NMOS region to form a peripheral NMOS transistor gate over the peripheral NMOS region, the peripheral NMOS transistor gate having opposing lateral sidewalls;

patterning the gate layer over the memory array region to form an array of memory NMOS transistor gates over the memory array region, the memory NMOS transistor gates having opposing lateral sidewalls;

while patterning the gate layer over the peripheral NMOS region, and while patterning the gate layer over the memory array region, leaving the gate layer over the PMOS region unpatterned;

providing sidewall spacers adjacent the sidewalls of the peripheral and memory NMOS transistor gates, the sidewall spacers having a lateral thickness and comprising a sidewall spacer material;

after providing the sidewall spacers forming electrically conductive peripheral NMOS source/drain regions within the semiconductor material operatively adjacent the peripheral NMOS transistor gate;

after forming the electrically conductive NMOS source/drain regions, etching the sidewall spacer material adjacent the peripheral NMOS transistor gate to remove only a portion of said spacer material and to thereby decrease the lateral thickness of the sidewall spacers adjacent the peripheral NMOS transistor gate; and

after decreasing the lateral thickness of the sidewall spacers adjacent the peripheral NMOS transistor gate, implanting conductivity-enhancing dopant into the semiconductor material to form peripheral NMOS graded junction regions operatively adjacent the peripheral NMOS transistor gate.

53. The method of claim 52 wherein the semiconductor material wafer comprises an overall planar global configuration, the planar global configuration establishing a virtual planar top surface and an axis normal to the virtual planar top surface, and wherein the p-type conductivity-enhancing dopant is implanted at an angle other than parallel to the axis normal to the virtual planar top surface.

54. The method of claim 52 wherein the implanted conductivity-enhancing dopant is a p-type dopant and wherein the formed NMOS graded junction regions are halo regions.

55. The method of claim 52 further comprising, after providing sidewall spacers adjacent the sidewalls of the peripheral and memory NMOS transistor gates, and prior to forming electrically-conductive NMOS source/drain regions, providing a masking layer over the memory array region.

56. The method of claim 52 further comprising, after providing transistor gates over the peripheral NMOS region and over the memory array region, and prior to providing sidewall spacers adjacent the sidewalls of the transistor gates, providing LDD regions operatively adjacent the peripheral NMOS transistor gate and providing source/drain regions operatively adjacent the memory NMOS transistor gates.

57. The method of claim 52 wherein the opposing lateral sidewalls of the peripheral and memory NMOS transistor gates comprise polysilicon, the method further comprising:

prior to providing sidewall spacers adjacent the sidewalls of the peripheral and memory NMOS transistor gates, oxidizing the polysilicon of the opposing lateral sidewalls to form an oxide layer along each of the opposing lateral sidewalls.

58. The method of claim 57 further comprising, prior to providing the oxide layer along each lateral sidewall of the peripheral and memory NMOS transistor gates, forming peripheral NMOS LDD

regions operatively adjacent the peripheral NMOS transistor gate and forming memory NMOS source/drain regions operatively adjacent the memory NMOS transistor gates.

59. The method of claim 52 further comprising:

after forming halo regions operatively adjacent the NMOS source/drain regions, providing a masking layer over the peripheral NMOS region;

after providing the masking layer over the peripheral NMOS region, patterning a PMOS transistor gate over the PMOS region; and

forming electrically conductive PMOS source/drain regions operatively adjacent the PMOS transistor gate.

60. The method of claim 59 further comprising forming PMOS graded junction regions operatively adjacent the PMOS source/drain regions.

61. The method of claim 59 further comprising forming PMOS graded junction regions operatively adjacent the PMOS source/drain regions, wherein the PMOS graded junction regions are formed after the PMOS source/drain regions are formed.

62. The method of claim 59 wherein the PMOS transistor gate has opposing lateral sidewalls, and further comprising:

providing sidewall spacers adjacent the sidewalls of the PMOS transistor gate, the sidewall spacers having a lateral thickness and comprising a sidewall spacer material;

after forming the electrically conductive PMOS source/drain regions, etching the sidewall spacer material adjacent the PMOS transistor gate to remove only a portion of said spacer material and to thereby decrease the lateral thickness of the sidewall spacers adjacent the PMOS transistor gate; and

after decreasing the lateral thickness of the sidewall spacers adjacent the PMOS transistor gate, implanting conductivity-enhancing dopant into the semiconductor material of the PMOS region to form PMOS graded junction regions operatively adjacent the PMOS transistor gate.

63. The method of claim 59 wherein the PMOS transistor gate has a top and pair of opposing lateral sidewalls, and further comprising:

providing an overhanging PMOS capping layer over the top of the PMOS transistor gate, the capping layer extending laterally outward beyond the pair of opposing lateral sidewalls;

after providing the capping layer, implanting p-type conductivity-enhancing dopant into the semiconductor material of the PMOS region to form the electrically conductive source/drain regions operatively adjacent the PMOS transistor gate, the overhanging capping layer offsetting the PMOS source/drain regions from the PMOS transistor gate;

removing the overhanging capping layer from the top of the PMOS transistor gate; and

implanting a conductivity-enhancing dopant into the semiconductor material of the PMOS region to form PMOS graded junction regions operatively adjacent the PMOS source/drain regions.

64. A method for forming graded junction regions operatively adjacent a transistor gate, the method comprising the following steps:

providing a semiconductor material wafer;

providing a transistor gate over the semiconductor material wafer, the transistor gate comprising a layer of polysilicon and having opposing lateral sidewalls which include an exposed portion of the layer of polysilicon;

forming an oxide layer along the exposed portion of the layer of polysilicon of the lateral sidewalls;

providing sidewall spacers adjacent the sidewalls of the transistor gate and adjacent the oxide layer, the sidewall spacers having a lateral thickness and comprising a sidewall spacer material;

after providing the sidewall spacers, implanting a first conductivity-enhancing dopant into the semiconductor wafer to form electrically conductive source/drain regions within the semiconductor material operatively adjacent the transistor gate;

after forming the electrically conductive source/drain regions, etching the sidewall spacer material adjacent the transistor gate to remove said sidewall spacers and to thereby expose the oxide layer; and

after exposing the oxide layer, implanting a second conductivity-enhancing dopant into the semiconductor material to form graded junction regions operatively adjacent the transistor gate.

65. The method of claim 64 further comprising, prior to forming the oxide layer along the exposed portion of the layer of polysilicon, forming graded junction regions operatively adjacent the transistor gate.

66. The method of claim 64 wherein the first conductivity-enhancing dopant is p-type, the second conductivity-enhancing dopant is n-type, and the implant of the second conductivity enhancing dopant forms halo regions.

67. The method of claim 64 wherein the first conductivity-enhancing dopant is p-type, the second conductivity-enhancing dopant is p-type, and the implant of the second conductivity enhancing dopant forms LDD regions.

68. The method of claim 64 wherein the first conductivity-enhancing dopant is n-type, the second conductivity-enhancing dopant is n-type, and the implant of the second conductivity enhancing dopant forms LDD regions.

69. The method of claim 64 wherein the first conductivity-enhancing dopant is n-type, the second conductivity-enhancing dopant is p-type, and the implant of the second conductivity enhancing dopant forms halo regions.

70. A method for forming a peripheral NMOS transistor and a memory array of NMOS transistors, the method comprising the following steps:

providing a semiconductor material wafer;

defining a memory array region, a PMOS region and a peripheral NMOS region of the wafer;

providing a gate layer over the PMOS, peripheral NMOS and memory array regions, the gate layer comprising a layer of polysilicon;

patterning the gate layer over the peripheral NMOS region to form a peripheral NMOS transistor gate, the peripheral NMOS transistor gate having opposing lateral sidewalls which include an exposed portion of the layer of polysilicon;

patterning the gate layer over the memory array region to form an array of memory NMOS transistor gates over the memory array region, the memory NMOS transistor gates having opposing lateral sidewalls which include an exposed portion of the layer of polysilicon;

while patterning the gate layer over the peripheral NMOS region, and while patterning the gate layer over the memory array regions, leaving the gate layer over the PMOS region unpatterned;

forming an oxide layer along the exposed portion of the layer of polysilicon of the lateral sidewalls of the peripheral NMOS transistor gate and along the exposed portions of the layer of polysilicon of the lateral sidewalls of the memory NMOS transistor gates;

providing sidewall spacers adjacent the sidewalls of the peripheral and memory NMOS transistor gates and adjacent the oxide layers;

after providing the sidewall spacers, forming electrically conductive peripheral NMOS source/drain regions within the semiconductor material operatively adjacent the peripheral NMOS transistor gate;

after forming the electrically conductive NMOS source/drain regions, removing the sidewall spacers from adjacent the peripheral NMOS transistor gate; and

after removing the sidewall spacers, implanting conductivity-enhancing dopant into the semiconductor material to form peripheral NMOS graded junction regions operatively adjacent the peripheral NMOS transistor gate.

71. The method of claim 70 further comprising, prior to forming the oxide layer along the exposed portion of the layer of polysilicon of the lateral sidewalls of the peripheral NMOS transistor gate and along the exposed portions of the layer of polysilicon of the lateral sidewalls of the memory NMOS transistor gates, providing peripheral NMOS LDD regions operatively adjacent the peripheral NMOS transistor gate and providing electrically-conductive memory array source/drain operatively adjacent the memory array transistor gates.

72. The method of claim 70 wherein the implant of conductivity-enhancing dopant into the semiconductor material comprises implanting p-type conductivity enhancing dopant and thereby forms peripheral NMOS halo regions operatively adjacent the peripheral NMOS transistor gate.

73. The method of claim 70 further comprising, prior to forming the oxide layer along the exposed portion of the layer of polysilicon of the lateral sidewalls of the peripheral NMOS transistor gate and along the exposed portions of the layer of polysilicon of the lateral sidewalls of the memory NMOS transistor gates, providing peripheral NMOS LDD regions operatively adjacent the peripheral NMOS transistor gate and providing electrically-conductive memory array source/drain operatively adjacent the memory array transistor gates; and wherein the implant of conductivity-enhancing dopant into the semiconductor material comprises implanting p-type conductivity enhancing dopant and thereby forms peripheral NMOS halo regions operatively adjacent the peripheral NMOS transistor gate.

74. The method of claim 70 further comprising, after providing sidewall spacers adjacent the sidewalls of the peripheral and memory NMOS transistor gates, and prior to forming electrically-conductive NMOS source/drain regions, providing a masking layer over the memory array region.

75. The method of claim 70 further comprising:

after forming peripheral NMOS graded junction regions operatively adjacent the NMOS source/drain regions, patterning a PMOS transistor gate over the PMOS region.

76. A method for forming a transistor device, the method comprising the following steps:

providing a semiconductor material wafer, the semiconductor wafer having a surface;

providing a transistor gate layer atop the surface of the semiconductor wafer, the transistor gate comprising an upper oxide layer and an insulative cap layer over the upper oxide layer, the upper oxide layer having an upper surface, the upper oxide upper surface being at a level above the surface of the semiconductor wafer, the insulative cap comprising an insulative cap material;

providing a masking layer over the transistor gate and over the surface of the semiconductor substrate, the masking layer having an upper surface and comprising a masking layer material;

removing masking layer material from over the transistor gate until the masking layer upper surface is about level with the level of the upper surface of the upper oxide layer; and

etching the insulative cap material to remove the insulative cap from over the transistor gate to thereby expose the upper surface of the upper oxide layer.

77. The method of claim 76 wherein the masking layer material comprises photoresist.

78. The method of claim 76 wherein the insulative cap material comprises silicon nitride.

79. The method of claim 76 wherein the transistor gate comprises opposing lateral sidewalls, the method further comprising:

after forming the transistor gate, providing sidewall spacers adjacent the opposing lateral sidewalls of the transistor gate, the sidewalls having a top surface, the top surface of the sidewall spacers being elevationally above the upper surface of the upper oxide layer; and

etching the sidewall spacers to form flat top surfaces of the sidewall spacers, the flat top surfaces being elevationally at about the same level as the exposed upper surface of the upper oxide layer of the transistor gate.

80. The method of claim 76 wherein the transistor gate comprises opposing lateral sidewalls, the method further comprising:

after forming the transistor gate, providing sidewall spacers adjacent the opposing lateral sidewalls of the transistor gate, the sidewalls having a top surface, the top surface of the sidewall spacers being elevationally above the upper surface of the upper oxide layer, the sidewall spacers comprising a sidewall spacer material which is identical to the material of the insulative cap; and

etching the sidewall spacer material to form flat top surfaces of the sidewall spacers, the flat top surfaces being elevationally at about the same level as the exposed upper surface of the upper oxide layer of the transistor gate, the etching of the sidewall spacer material occurring concurrently with the etching of the insulative cap material.

81. The method of claim 80 wherein the insulative cap material and the sidewall spacer material both comprise silicon nitride.

82. A method for forming CMOS circuitry, the method comprising the following steps:

providing a semiconductor material wafer, the semiconductor wafer having a surface;

defining a PMOS region and an NMOS region of the wafer;

providing a gate layer over the PMOS region and over the NMOS region, the gate layer having an upper oxide layer and an insulative cap over the upper oxide layer, the upper oxide layer having an upper surface, the upper oxide upper surface being at a level above the surface of the semiconductor wafer, the insulative cap comprising an insulative cap material;

patterning the gate layer over the NMOS region to form an NMOS transistor gate over the NMOS region while leaving the gate layer over the PMOS region unpatterned;

providing a masking layer over the PMOS region and the NMOS region, the masking layer having an upper surface and comprising a masking layer material;

removing masking layer material from over the PMOS and NMOS regions until the masking layer upper surface is about level with the level of the upper surface of the upper oxide layer; and

etching the insulative cap material to remove the insulative cap from over the NMOS gate and from over the unpatterned gate layer over the PMOS region to thereby expose the upper surface of the upper oxide layer of the NMOS gate and to also thereby expose the

upper surface of the upper oxide layer of the unpatterned gate layer over the PMOS region.

83. The method of claim 82 wherein the masking layer material comprises photoresist.

84. The method of claim 82 wherein the insulative cap material comprises silicon nitride.

85. The method of claim 82 wherein the NMOS transistor gate comprises opposing lateral sidewalls, the method further comprising:

after forming the NMOS transistor gate, providing sidewall spacers adjacent the opposing lateral sidewalls of the NMOS transistor gate, the sidewalls having a top surface, the top surface of the sidewall spacers being elevationally above the upper surface of the upper oxide layer; and

etching the sidewall spacers to form flat top surfaces of the sidewall spacers, the flat top surfaces being elevationally at about the same level as the exposed upper surface of the upper oxide layer of the NMOS gate.

86. The method of claim 82 wherein the NMOS transistor gate comprises opposing lateral sidewalls, the method further comprising:

after forming the NMOS transistor gate, providing sidewall spacers adjacent the opposing lateral sidewalls of the NMOS transistor gate, the sidewalls having a top surface, the top surface of the sidewall spacers being elevationally above the upper surface of the upper oxide layer, the sidewall spacers comprising a sidewall spacer material which is identical to the material of the insulative cap; and

etching the sidewall spacer material to form flat top surfaces of the sidewall spacers, the flat top surfaces being elevationally at about the same level as the exposed upper surface of the upper oxide layer of the NMOS gate, the etching of the sidewall spacer material occurring concurrently with the etching of the insulative cap material.

87. The method of claim 86 wherein the insulative cap material and the sidewall spacer material both comprise silicon nitride.

88. A method for forming an NMOS transistor device and an insulated word line, the method comprising the following steps:

providing a semiconductor material wafer, the semiconductor wafer having a surface;

defining a memory array region of the wafer and a peripheral NMOS region of the wafer;

providing a gate layer over the peripheral NMOS and memory array regions of the wafer, the gate layer having an upper oxide layer and an insulative cap over the upper oxide layer, the upper oxide layer having an upper surface, the upper oxide layer upper surface being at a level above the surface of the semiconductor wafer, the insulative cap comprising an insulative cap material;

patterning the gate layer over the peripheral NMOS region to form a peripheral NMOS transistor gate over the peripheral NMOS region, the peripheral NMOS transistor gate having opposing lateral sidewalls;

patterning the gate layer over the memory array region to form a word line, the word line having opposing lateral sidewalls;

providing insulative sidewall spacers adjacent the opposing lateral sidewalls of the peripheral NMOS transistor gate and adjacent the opposing lateral sidewalls of the word line, the sidewall spacers comprising a sidewall spacer material;

providing a masking layer over the peripheral NMOS region, the masking layer having an upper surface and comprising a masking layer material;

removing the masking layer material from over peripheral NMOS region until the masking layer upper surface is about level with the upper oxide layer upper surface; and

removing the insulative cap material from over the peripheral NMOS transistor gate to expose the upper oxide upper surface of the peripheral NMOS gate.

89. The method of claim 88 further comprising:

prior to removing the masking layer material from over the peripheral NMOS transistor gate, providing a masking layer over the word line, the masking layer over the word line comprising a masking layer material identical to the masking material of the masking layer over the peripheral NMOS transistor gate, the masking layer material over the word line having an upper surface which is elevationally above the upper surface of the masking material over the peripheral NMOS transistor gate; and

wherein the step of removing the masking layer material from over peripheral NMOS region leaves masking layer material over the word line.

90. The method of claim 88 further comprising:

prior to removing the insulative cap from over the peripheral NMOS transistor gate, providing a masking layer over the word line.

91. The method of claim 88 further comprising:

defining a PMOS region of the semiconductor material wafer;

providing the gate layer over the PMOS region;

while patterning the gate layer over the peripheral NMOS region, and while patterning the gate layer over the memory array region, leaving the gate layer over the PMOS region unpatterned; and

while providing the masking layer over the peripheral NMOS region, also providing the masking layer over the PMOS region.

92. The method of claim 88 further comprising:

defining a PMOS region of the semiconductor material wafer;

providing the gate layer over the PMOS region;

while patterning the gate layer over the peripheral NMOS region, and while patterning the gate layer over the memory array region, leaving the gate layer over the PMOS region unpatterned;

while providing the masking layer over the peripheral NMOS region, also providing the masking layer over the PMOS region;

wherein the step of removing the masking layer material from over peripheral NMOS region also removes masking layer material from over the PMOS region; and

wherein the step of removing the insulative cap material from over the peripheral NMOS transistor gate to expose the upper oxide upper surface of the peripheral NMOS gate also removes insulative cap material from over the PMOS region to expose an upper oxide surface of the unpatterned masking material over the PMOS region.

93. The method of claim 88 wherein the sidewall spacers of the peripheral NMOS transistor have a top surface, the top surfaces of the sidewall spacers being elevationally above the upper surface of the upper oxide layer of the peripheral NMOS transistor, the method further comprising:

etching the sidewall spacers of the peripheral NMOS transistor to form flat top surfaces of the sidewall spacers of the peripheral NMOS transistor, the flat top surfaces being elevationally at about the same level as the exposed upper surface of the upper oxide layer of the peripheral NMOS gate.

94. The method of claim 88 wherein the sidewall spacers of the peripheral NMOS transistor have a top surface, the top surfaces of the sidewall spacers being elevationally above the upper surface of the upper oxide layer of the peripheral NMOS transistor, the method further comprising:

etching the sidewall spacer material of the peripheral NMOS transistor to form flat top surfaces of the sidewall spacers of the peripheral NMOS transistor, the flat top surfaces being elevationally at about the same level as the exposed upper surface of the upper oxide layer of the peripheral NMOS gate, the etching of the sidewall spacer material occurring concurrently with the etching of the insulative cap material.

95. The method of claim 88 further comprising patterning the gate layer over the memory array region to form memory transistor gates.

96. The method of claim 88 wherein the insulative cap material and the sidewall spacer material both comprise silicon nitride.

97. A method for forming a PMOS transistor device, a peripheral NMOS transistor device, and one or more memory NMOS transistor devices, the method comprising the following steps:

providing a semiconductor material wafer;

defining a PMOS region, a peripheral NMOS region, and a memory array region of the wafer;

providing a gate layer over the PMOS, peripheral NMOS and memory array regions;

patterning the gate layer over the peripheral NMOS region to form a peripheral NMOS transistor gate;

patterning the gate layer over the memory array region to form one or more memory array transistor gates;

while patterning the gate layer over the peripheral NMOS and memory array regions, leaving the gate layer over the PMOS region unpatterned;

forming source/drain regions, halo regions and LDD regions operatively adjacent the peripheral NMOS transistor gate, and forming source/drain regions operatively adjacent the one or more memory NMOS transistor gates, the steps of forming the regions occurring in a sequence such that one or more of the regions are formed last and are therefore last formed regions; and

less than two masking layer provision steps after the formation of the peripheral NMOS transistor gate, and prior to the formation of the one or more last formed regions.

98. A method of forming a transistor structure on a semiconductor substrate, comprising the following steps:

providing a transistor gate assembly formed on said substrate, said gate assembly including sidewall spacers extending to said substrate;

doping a first region of said substrate with a selected dopant;

removing a lateral portion of at least one of said sidewall spacers, while leaving a part of said at least one of said sidewall spacers in place; and

after said removal, doping a second portion of said substrate.